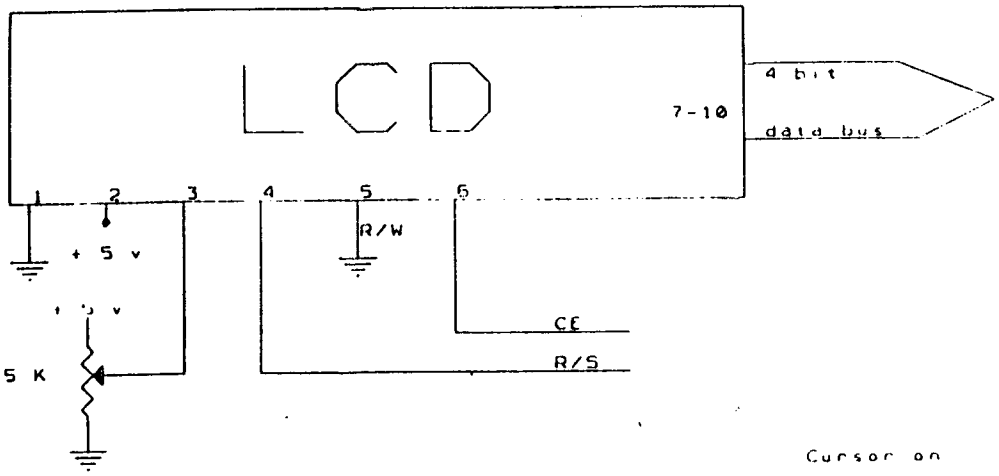
2 LINE BY 20 CHARACTER

Front View

Back Light

10 9 8 7 6 5 4 3 2 1

1. Gnd 2. Vcc 3. Vee 4. R/S 5. R/W 6. CE 7. DB-4 8. DB-5 9. DB-6 10. DB-7



Initialization Sequence

	R/S	DB7	DB6	DB5	DB4	HEX	CE
	0	0	0	1	1	3	
	0	0	0	1	1	3	
	0	0	0	1	1	3	
	0	0	0	1	0	2	
	0	0	0	1	0	2	
	0	1	0	0	0	8	
	0	0	0	0	0	0	
	0	1	0	0	0	8	
	0	0	0	0	0	0	
	0	0	0	0	1	1	
	0	0	0	0	0	0	
Cursor on	0	1	1	0	1	D	

All data must be written twice ... upper nibble 1st

01 Clears entire display & places cursor on line position 1

C0H positions cursor at the start of line 2

*Other functions can be found in OPTREX data sheet *

Danny Morse DeVRY Institute		
Size	Document Number	REV
A	LCD Data Sheet	A
Date: August 10, 1991	Sheet 1 of 1	

16 x 2 [redacted]
4A4

USING HD44780A00H

PINOUT

DB6	02	10	DB7
DB4	0	0	DB5
DB2	0	0	DB3
DB0	0	0	DB1
R/$\bar{W}$	0	0	EN
VLCD	0	0	RS (DATA/$\overline{CMD}$)
VCC	01M	130	VSS (GND)

VLCD - LCD DRIVE VOLTAGE

→ 0 - 5V

DO NOT EXCEED!

SET UP R/$\bar{W}$, RS

Then pulse EN ⊓ FOR 1mS

INITIALIZATION

For 8 bit data interfacing

Power On

Wait for 15ms or more after Vcc rises to 4.5V

BF cannot be checked at this time

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Ø	Ø	Ø	Ø	1	1	X	X	X	X

Function set : DL=1, 8 bit interface data.
DL must set at H during this initialzation.

Wait for 4.1 ms or more

BF cannot be checked at this time

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Ø	Ø	Ø	Ø	1	1	X	X	X	X

Function set : DL=1, 8 bit interface data.
DL must set at H during this initialzation.

Wait for 100μs or move

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Ø	Ø	Ø	Ø	1	1	X	X	X	X

Function set : DL=1, 8 bit interface data.
DL must set at H during this initialzation.

BF can be checked at this time, check for not busy

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Ø	Ø	Ø	Ø	1	1	N	F	X	X

Function set : DL=1, 8 bit interface data.
N = no.of line
F = character font

check for not busy

Ø	Ø	Ø	Ø	Ø	Ø	1	Ø	Ø	Ø

Display off

check for not busy

Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1

Clears all display and return cursor to home position

check for not busy

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	I/D	S

Set the shift mode *

End of initialization

*NOTE : IN NORMAL OPERATION, SET S TO Ø

For 4 bit data interfacing

Power On

Wait for 15ms or more after Vcc rises to 4.5V

BF cannot be checked at this time

RS	R/W	DB7	DB6	DB5	DB4
Ø	Ø	Ø	Ø	1	1

Function set : DL=1, 8 bit interface data.
DL must set at H during this initialzation.

Wait for 4.1 ms or more

BF cannot be checked at this time

RS	R/W	DB7	DB6	DB5	DB4
Ø	Ø	Ø	Ø	1	1

Function set : DL=1, 8 bit interface data.
DL must set at H during this initialzation.

Wait for 100μs or more

BF can be checked at this time

RS	R/W	DB7	DB6	DB5	DB4
Ø	Ø	Ø	Ø	1	1

Function set : DL=1, 8 bit interface data.
DL must set at H during this initialzation.

check for not busy

RS	R/W	DB7	DB6	DB5	DB4
Ø	Ø	Ø	Ø	1	Ø

Function set : DL=Ø, 4 bit interface data.

check for not busy

RS	R/W	DB7	DB6	DB5	DB4
Ø	Ø	Ø	Ø	1	Ø
Ø	Ø	N	F	X	X

Function set : DL=Ø, 4 bit interface data.
N = no. of line
F = character font

check for not busy

RS	R/W	DB7	DB6	DB5	DB4
Ø	Ø	Ø	Ø	Ø	Ø
Ø	Ø	1	Ø	Ø	Ø

Display off

check for not busy

RS	R/W	DB7	DB6	DB5	DB4
Ø	Ø	Ø	Ø	Ø	Ø
Ø	Ø	Ø	Ø	Ø	1

Display on

check for not busy

RS	R/W	DB7	DB6	DB5	DB4
Ø	Ø	Ø	Ø	Ø	Ø
Ø	Ø	Ø	1	I/D	S

Entry mode set *

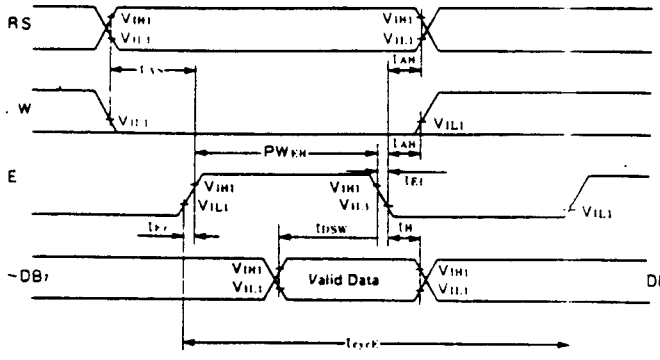
End of initialization

TIMING CHART

Item	Symbol	Measuring Condition	Standard Value			Unit
			min.	typ.	max.	
Enable Cycle Time	TcycE	Figs. 1, 2	1000	—	—	nS
Enable Pulse Width, High Level	PWEH	Figs. 1, 2	450	—	—	nS
Enable Rise and Decay Time	tEr, tEf	Figs. 1, 2	—	—	25	nS
Address Setup Time, RS, R/W – E	tAS	Figs. 1, 2	140	—	—	nS
Data Delay Time	tDDR	Fig. 2	—	—	320	nS
Data Setup Time	tDSW	Fig. 1	195	—	—	nS
Data Hold Time	tH	Fig. 1	10	—	—	nS
Data Hold Time	tDHR	Fig. 2	20	—	—	nS
Address Hold Time	tAH	Figs. 1, 2	10	—	—	nS

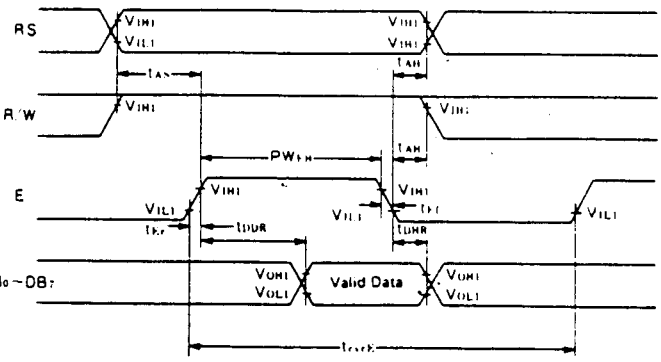
* Vcc = 5.0V ± 5%, Ta = 25°C

FIG. 1 WRITE OPERATION



(Write Data from MPU to MODULE)

FIG. 2 READ OPERATION



(Reading Data from MODULE to MPU)

PIN ASSIGNMENT

Pin No.	Symbol	Level	Function	
1	Vss	—	Power Supply	0V (GND)
2	Vcc	—		+ 5 V
3	Vee	—		for Liquid Crystal Drive
4	RS	H/L	Register H: Data Input Select L: Instruction Input	
5	R/W	H/L	H: Data Read (Module→MPU) L: Data Write (Module←MPU)	
6	E	H,H←L	Enable Signal	
7	DB 4	H/L	Data Bus Line	
8	DB 5	H/L		
9	DB 6	H/L		
10	DB 7	H/L		

■ In the data bus line, data transfer is performed two times by the 4-bit or one time by the 8-bit in order to interface with 4-bit or 8-bit MPU.

■ In case interface data length is 4-bit. The data is transferred by using only four buses of DB4 ~ DB7 and the buses of DB0 ~ DB3 are not used. The data transfer to MPU is completed by transferring the data of 4-bits twice. Transfer of upper four bits and low four bits is performed in sequence.

■ In case interface data length is 8-bit. Data transfer is performed by using eight buses of DB0 ~ DB7.

DISPLAY CHARACTER POSITION AND DD RAM ADDRESS (CONTINUE)

2x16 DMM, 1/16 MUX

N=1 : 2-LINE DISPLAY F=Ø : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← DISPLAY POSITION
FIRST LINE	ØØ	Ø1	Ø2	Ø3	Ø4	Ø5	Ø6	Ø7	Ø8	Ø9	ØA	ØB	ØC	ØD	ØE	ØF	← DD RAM ADDRESS
SECOND LINE	4Ø	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

WHEN THE DISPLAY SHIFT OPERATION IS PERFOMED, THE DD RAM ADDRESS MOVED AS FOLLOW :

AFTER THE LEFT SHIFT INSTRUCTION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← DISPLAY POSITION
	Ø1	Ø2	Ø3	Ø4	Ø5	Ø6	Ø7	Ø8	Ø9	ØA	ØB	ØC	ØD	ØE	ØF	1Ø	← DD RAM ADDRESS
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	5Ø	

AFTER THE RIGHT SHIFT INSTRUCTION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← DISPLAY POSITION
	27	ØØ	Ø1	Ø2	Ø3	Ø4	Ø5	Ø6	Ø7	Ø8	Ø9	ØA	ØB	ØC	ØD	ØE	← DD RAM ADDRESS
	67	4Ø	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

2x20 DMM, 1/16 MUX

N=1 : 2-LINE DISPLAY F=Ø : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	← DISPLAY POSITION
FIRST LINE	ØØ	Ø1	Ø2	Ø3	Ø4	Ø5	Ø6	Ø7	Ø8	Ø9	ØA	ØB	ØC	ØD	ØE	ØF	1Ø	11	12	13	← DD RAM ADDRESS
SECOND LINE	4Ø	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	5Ø	51	52	53	

2x24 DMM, 1/16 MUX

N=1 : 2-LINE DISPLAY F=Ø : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	← DISPLAY POSITION
FIRST LINE	ØØ	Ø1	Ø2	Ø3	Ø4	Ø5	Ø6	Ø7	Ø8	Ø9	ØA	ØB	ØC	ØD	ØE	ØF	1Ø	11	12	13	14	15	16	17	← DD RAM ADDRESS
SECOND LINE	4Ø	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	5Ø	51	52	53	54	55	56	57	

2x40 DMM, 1/16 MUX

N=1 : 2-LINE DISPLAY F=Ø : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	...	33	34	35	36	37	38	39	40	← DISPLAY POSITION
FIRST LINE	ØØ	Ø1	Ø2	Ø3	Ø4	Ø5	Ø6	Ø7	Ø8	Ø9	ØA	ØB	ØC		2Ø	21	22	23	24	25	26	27	← DD RAM ADDRESS
SECOND LINE	4Ø	41	42	43	44	45	46	47	48	49	4A	4B	4C		6Ø	61	62	63	64	65	66	67	

4x16 DMM, 1/16 MUX

N=1 : 2-LINE DISPLAY F=Ø : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← DISPLAY POSITION
FIRST LINE	ØØ	Ø1	Ø2	Ø3	Ø4	Ø5	Ø6	Ø7	Ø8	Ø9	ØA	ØB	ØC	ØD	ØE	ØF	← DD RAM ADDRESS
SECOND LINE	4Ø	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	
THIRD LINE	1Ø	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	
FOURTH LINE	5Ø	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	

4x40 DMM, 1/16 MUX

N=1 : 2-LINE DISPLAY F=Ø : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	← DISPLAY POSITION
FIRST LINE	ØØ	Ø1	Ø2	Ø3	Ø4	Ø5	Ø6	Ø7	Ø8	Ø9	ØA	ØB	ØC	ØD	ØE	ØF	1Ø	11	12	13	← DD RAM ADDRESS
SECOND LINE	4Ø	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	5Ø	51	52	53	
THIRD LINE	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	2Ø	21	22	23	24	25	26	27	
FOURTH LINE	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	6Ø	61	62	63	64	65	66	67	

INSTRUCTION SET

INSTRUCTION	CODE										DESCRIPTION	TYPICAL EXECUTION TIME
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	Clears display and returns the cursor to home position (Address Ø). Sets I/D=1 of Entry Mode.	1.64 ms
Return home	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	●	Return the cursor to the home position (Address Ø). Also returns the display being shifted to the original position. DD RAM contents remain unchanged. Set DD RAM addresses to zero.	1.64 ms
Entry mode set	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	I/D	S	Set the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read of DD RAM/CG RAM. FOR NORMAL OPERATION, SET S TO Ø	40 µs
Display ON/Off control	Ø	Ø	Ø	Ø	Ø	Ø	1	D	C	B	Sets ON/OFF all display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40 µs
Cursor or display shift	Ø	Ø	Ø	Ø	Ø	1	S/C	R/L	●	●	Moves the cursor and shifts the display without changing DD RAM contents.	40 µs
Function set	Ø	Ø	Ø	Ø	1	DL	N	F	●	●	Sets interface data length (DL) number of display lines (N) and character font (F).	40 µs
Set the CG RAM address	Ø	Ø	Ø	1	MSB	ACG				LSB	Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 µs
Set the DD RAM address	Ø	Ø	1	MSB	ADD					LSB	Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 µs
Read busy flag & address	Ø	1	BF	MSB	AC					LSB	Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	40 µs
Write data to CG or DD RAM	1	Ø	MSB							LSB	Writes data into DD RAM or CG RAM.	40 µs
Read data from CG or DD RAM	1	1	MSB							LSB	Reads data from DD RAM or CG RAM.	40 µs
	S =1: Accompanies display shift when data is written. for normal operation, set to Ø I/D=1: Increment I/D=Ø: Decrement S/C=1: Display shift S/C=Ø: Cursor move R/L=1: Shift to the right R/L=Ø: Shift to the left BF =1: Internally operating BF =Ø: Can accept instruction						DL=1 : 8 bits DL=Ø : 4 bits N =1 : 2 (1) line N =Ø : 1 line F =1 : 5x1Ø dots F =Ø : 5x7 dots				DD RAM : Display data RAM CG RAM : Character generator RAM ACG : CG RAM address ADD : DD RAM address corresponds to cursor address AC : Address counter used for both DD and CG RAM address B : 1=ON Ø=OFF (Blinking cursor) C : 1=ON Ø=OFF (Cursor) D : 1=ON Ø=OFF (Display) ● Don't Care	

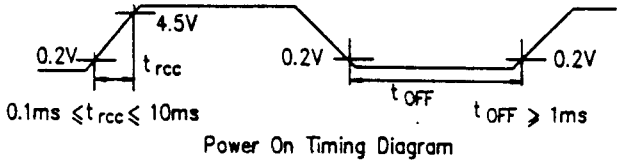
INITIALIZATION

The module automatically performed initialization when powered on (using internal reset circuit). The following instructions are executed during initialization :-

1. CLEAR DISPLAY
   The Busy Flag is kept in the Busy State (BF=1) unit initialization ends. The time is 15 ms.
2. Function Set ---------- DL= 1: 8-bits long interface data
   N = Ø : 1 Line display
3. DISPLAY ON/OFF CONTROL--- D = Ø : Display OFF
   C = Ø : Cursor OFF
   B = Ø : Blink OFF
4. ENTRY MODE SET -------- I/D= 1 : +1(INCREMENT)
   S = Ø : NO SHIFT
5. DD RAM IS SELECTED

Power On Initialization depends on rise time of the supply when it is turned on. The following time relationship must be satisfied.

ITEM	SYMBOL	STANDARD TIME			UNIT
		MIN	TYP	MAX	
Power Supply Rise Time	t_{rcc}	Ø.1	-	1Ø	ms



Power On Timing Diagram

NOTE :
When the above power supply condition is not satisfied, the internal reset circuitry does not operate correctly. In this case, perform the needed initialization by sending function set instructions thrice from MPU after turning the power on. For example, to designate a 8-bits data length, send the following instructions thrice.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Ø	Ø	Ø	Ø	1	1	●	●	●	●
Ø	Ø	Ø	Ø	1	1	●	●	●	●
Ø	Ø	Ø	Ø	1	1	●	●	●	●

When this ends, the module enters 8-bits data length mode without fail. then enter 4-bits data length instruction for 4-bits data