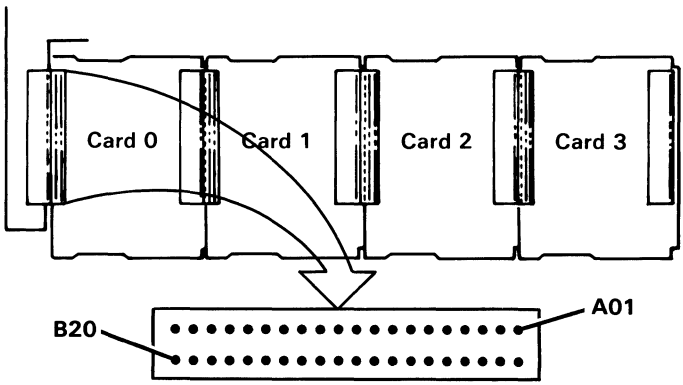
Random Access Memory (RAM)

The RAM is used to store application programs and user data. All RAM is static and does not require refresh. RAM does not use parity. The RAM is contained on cards; each card has 128K bytes of storage. A maximum of four cards can be installed in the system.

The starting address of RAM is hex 00000, as shown in Figure 2-3 on page 2-6. Figure 2-13 on page 2-34 shows the expansion RAM connectors at the system board. The plus (+) or minus (−) preceding the signal name indicates the active state of the signals. The input/output column indicates whether the signal direction is to or from the system board.



I/O Pin	Signal Name	Input/Output
A01	+Address/Data Bit 0	Input/Output
A02	+Address/Data Bit 1	Input/Output
A03	+Address/Data Bit 2	Input/Output
A04	+5 V dc	Power
A05	+Address/Data Bit 3	Input/Output
A06	+Address/Data Bit 4	Input/Output
A07	+Address/Data Bit 5	Input/Output
A08	+5 V dc	Power
A09	+Address/Data Bit 6	Input/Output
A10	+Address/Data Bit 7	Input/Output
A11	+Address Bit 8	Output
A12	+5 V dc	Power
A13	+Address Bit 9	Output
A14	+Address Latch Enable	Output
A15	Reserved	
A16	+5 V dc	Power
A17	−Memory Card Select 0	Output
A18	−Memory Card Select 2	Output
A19	−Memory Card Select 3	Output
A20	−Memory Card Select 4	Output
B01	+A10	Output
B02	Ground	Ground
B03	+Address Bit 11	Output
B04	Ground	Ground
B05	+Address Bit 12	Output
B06	Ground	Ground
B07	+Address Bit 13	Output
B08	Ground	Ground
B09	+Address Bit 14	Output
B10	Ground	Ground

Figure 2-13 (Part 1 of 2). System Board RAM Connector

I/O Pin	Signal Name	Input/Output
B11	+Address Bit 15	Output
B12	Ground	Ground
B13	+Address Bit 16	Output
B14	Ground	Ground
B15	−Memory Write	Output
B16	−Data Enable	Output
B17	−Memory Card Select 1	Output
B18	Ground	Ground
B19	+RAM Enable	Output
B20	Ground	Ground

Figure 2-13 (Part 2 of 2). System Board RAM Connector

The following is a description of the signals on the RAM connectors.

Address/Data Bit 0 through 7

These multiplexed lines are used to form either the low-order bits of an address or a byte of data. At the falling edge of the 'address latch enable' signal, the RAM cards access these eight lines along with lines 'address bit 8' through 'address bit 16' to form an address. At the low level of either 'memory read' or 'memory write', the RAM cards access these eight lines to form a data byte. The least significant bit is 'address/data bit 0.'

Address Bit 8 through 16

These lines are used to address memory and I/O devices within the system. The data on these lines is valid through the entire bus cycle.

Memory Card Select 0 through 4

These lines are used to select the card to be accessed. These lines are shifted at the output of the RAM cards.

Address Latch Enable

This line is used to indicate that the address/data bus contains a valid address.

Memory Write

This line is used to instruct a RAM card to store the data present on the data bus.

Data Enable

This line indicates when data should be gated onto the multiplexed address/data bus.

RAM Enable

This line enables the RAM card to be accessed. When this line is low, all other signals to the card are ignored.

I/O Channel

The I/O channel is an extension of the internal bus used by the processor and other functional units in the IBM PC Convertible. The channel contains multiplexed low-order address/data lines (bidirectional), high-order address lines, six interrupt control lines, memory and I/O read or write control lines, clock and timing lines, three DMA control lines, a channel-check line, and power and ground lines for the optional features. A serial printer interface for the IBM PC Convertible Portable Printer is also provided on the I/O channel connector.