PNP
MJ2501
NPN
MJ3001

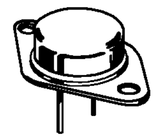
Motorola Preferred Devices

Medium-Power Complementary Silicon Transistors

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — h_{FE} = 4000 (Typ) @ I_C = 5.0 Adc
- Monolithic Construction with Built–in Base–Emitter Shunt Resistors

10 AMPERE DARLINGTON POWER TRANSISTOR COMPLEMENTARY SILICON 80 VOLTS 150 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Base Voltage	V_{CB}	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	0.2	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

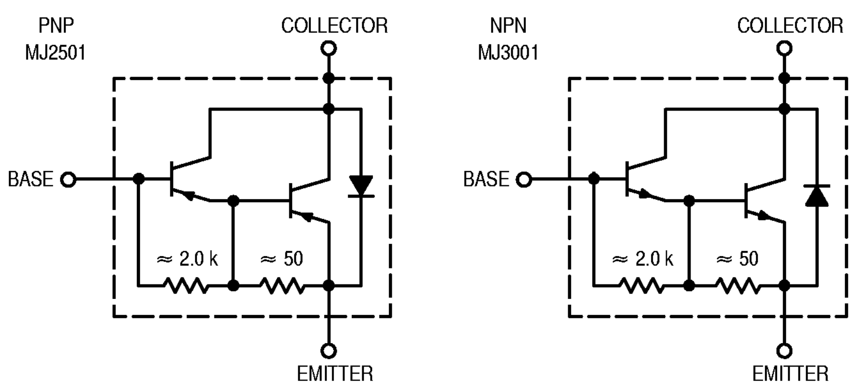


Figure 1. Darlington Circuit Schematic

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	80	—	Vdc
Collector–Emitter Leakage Current (V_{EB} = 80 Vdc, R_{BE} = 1.0 k ohm) (V_{EB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	I_{CER}	— —	1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mAdc
Collector Emitter Leakage Current (V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
ON CHARACTERISTICS(1)				
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	1000	—	—
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 20 mAdc) (I_C = 10 Adc, I_B = 50 mAdc)	$V_{CE(sat)}$	— —	2.0 4.0	Vdc
Base Emitter Voltage (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	$V_{BE(on)}$	—	3.0	Vdc

(1)Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

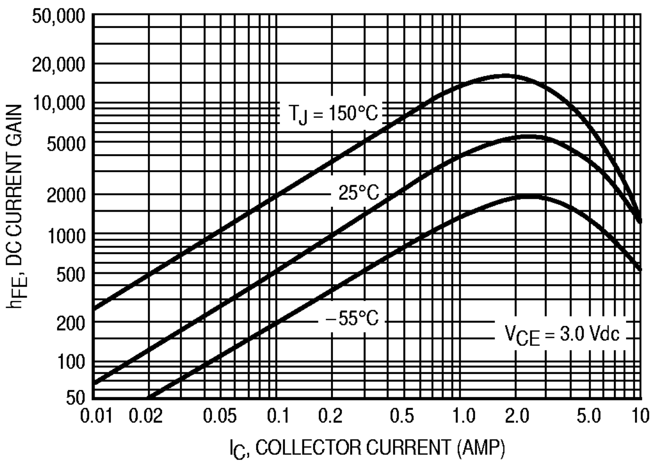


Figure 2. DC Current Gain

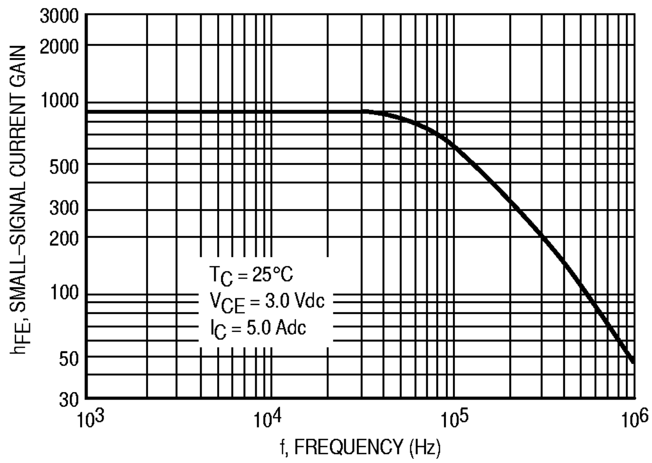


Figure 3. Small–Signal Current Gain

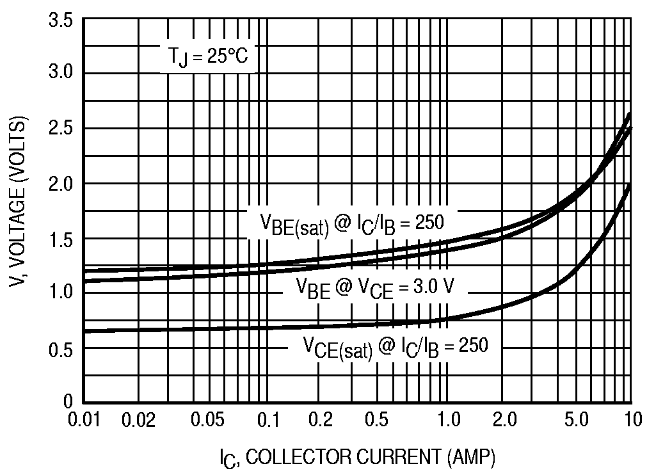


Figure 4. "On" Voltages

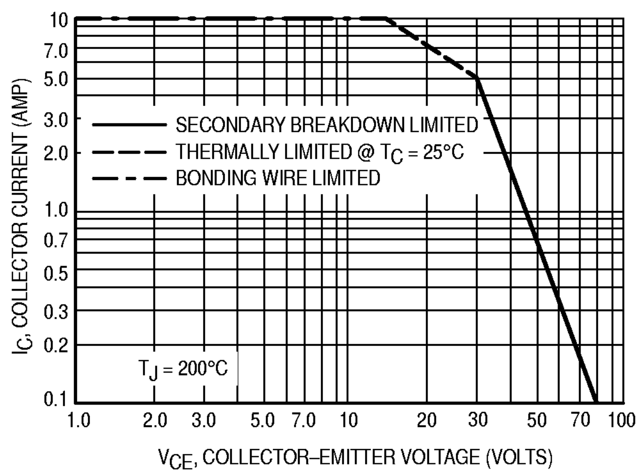
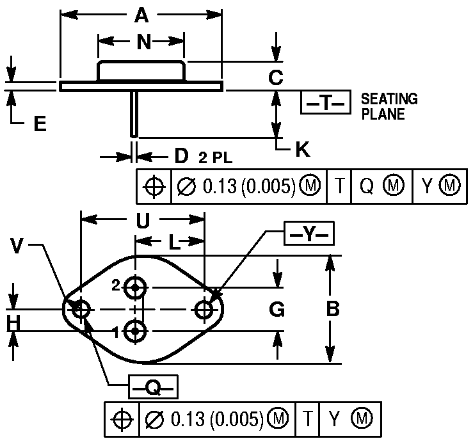


Figure 5. DC Safe Operating Area

There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1–07
TO–204AA (TO–3)
ISSUE Z